

Optical Interconnect with Densely Integrated Plasmonic Modulator and Germanium Photodetector Arrays

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Abstract: We demonstrate the first chip-to-chip interconnect utilizing a densely integrated plasmonic Mach-Zehnder modulator array operating at 3×10 Gbit/s. A multicore fiber provides a compact optical interface, while the receiver consists of germanium photodetectors.

OCIS codes: (200.4650) Optical interconnects, (250.5403) Plasmonics, (250.4110) Modulators, (230.0040) Detectors

1. Introduction

Optical interconnects offer the high-speed capabilities needed to cope with the continuously increasing bandwidth requirements [1]. To be a practical solution, they must further offer ultra-dense on-chip integration. In the past years, compact receiver solutions have indeed been demonstrated; e.g. based on germanium (Ge) detectors offering 56 Gbit/s operation [2]. Another challenge towards dense integration is the fiber-to-chip interface. Fiber ribbons, however, come at a typical channel spacing of 125 μm . And while plastic interconnects provide a smaller channel spacing (62.5 μm), they are used for short distances only [3]. As an alternative, multicore fibers (MCF) have been proposed, offering both a small channel spacing and transmission over long distances [4]. Yet, the biggest challenge so far remains the transmitter. Unless integrated into resonant structures, the footprint of state-of-the-art silicon photonic modulators is far too large for dense transmitters [5]. Recently, plasmonic solutions for compact electro-optic devices have emerged [6]. Only recently, we have demonstrated micrometer sized plasmonic modulators in a Mach-Zehnder configuration with line rates up to 108 Gbit/s [7, 8].

In this paper, we show the first chip-to-chip interconnect relying on a compact plasmonic transmitter (Tx). The transmitter consists of a plasmonic Mach-Zehnder modulator (MZM) array packaged with its driving electronics. The size of the MZM array with 12.5 μm long phase shifters is only dictated by the size of the electrical contact pads. Light from an external laser source is fed to the transmitter via a MCF providing a channel spacing of only 50 μm . On the receiver side, a Ge photodetector array was integrated together with trans-impedance amplifiers. Finally, chip-to-chip interconnect operation at 3×10 Gbit/s is demonstrated.

2. Transmitter

The plasmonic transmitter is shown in Fig. 1(a). A customized housing was fabricated in-house to assemble the photonic chip with the plasmonic MZM array on it and its driving electronics via wire bonding. The data signals were fed to the transmitter via high-speed K-connectors at the edge of the housing. The driving RF signals were amplified by four amplifiers (Amp) mounted on a printed circuit board (PCB). To minimize the length of the wire bonds, the photonic chip was placed in a cavity in the middle of the housing, while providing two RF signals from each side. The housing was mounted on a copper block that acted both as an external heat sink to dissipate the heat from the RF amplifiers, and also to adjust the height of the sample to our characterization setup. No active cooling is required to operate the transmitter. Light was coupled in and out of the photonic chip via silicon grating couplers (GCs) matched to a multicore fiber (MCF) and a standard single mode fiber (SMF), respectively. The plasmonic modulator array is shown in Fig. 1(b) and described in detail in Ref. [9]. It consists of 12.5 μm long plasmonic phase shifters, see inset (I), that are arranged in an imbalanced silicon Mach-Zehnder interferometer configuration. The distance between two adjacent MZMs of 300 μm is only limited by the size of the electrical contact pads needed for wire bonding. Inset (II) shows the facet of the MCF with a 50 μm channel spacing. Once electronics and plasmonics are integrated onto the same chip, so that contact pads are not needed any more, one can imagine to squeeze the plasmonic MZMs between the cores of the MCFs.

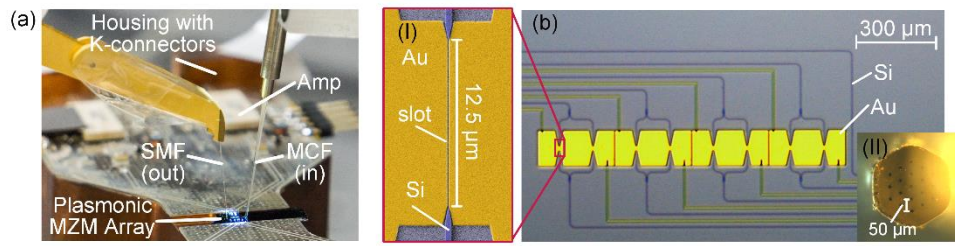


Fig. 1 Plasmonic transmitter (Tx). (a) Customized package with plasmonic modulator array and PCB containing driving electronics. (b) Plasmonic MZM array with silicon (Si) interferometers according to [9]. Inset (I) shows a zoom-in of the plasmonic phase shifter consisting of two gold (Au) electrodes being separated by a 75 nm wide and 12.5 μm long slot that is filled with an organic second-order nonlinear optical material. Inset (II) shows the facet of the multicore fiber (MCF) with a channel spacing of 50 μm matched to silicon grating couplers.

The driving electronics were tested using RF probes before bonding to the plasmonic modulators. Measurements of the S-parameters showed that the amplifiers provide ~ 25 dB gain at 10 GHz, while the input reflection coefficient is better than -6 dB up to 40 GHz. Data experiments at 10 Gbit/s (NRZ, pulse shape square-root-raised cosine SRRC, roll off $\alpha = 0.35$, De Bruijn bit sequences DBBS 15, 500 mV_{pp} input signal) show open eye diagrams for all amplifiers with quality factors Q^2 of 15.9 dB, 14.8 dB, 16.8 dB, 16.7 dB for channel 1, 2, 3, 4, respectively.

The plasmonic transmitter was verified by data modulation experiments. Laser light at $\lambda \approx 1550$ nm was coupled to the array via the MCF. Two digital-to-analog converters (72 GSa/s, 6 bit) generated uncorrelated, differential signals D_1 and D_2 at 10 Gbit/s (binary phase shift keying (BPSK), SRRC, $\alpha = 1$, DBBS 11). D_1, D_2, D_1 , and D_2 were fed to the single ended transmitter. The four channels were received sequentially with a standard SMF in a coherent receiver. Pre-distortion and post-equalization of the electrical signal was used to mitigate the frequency dependence of the driving electronics. Fig. 2 depicts the measured optical eye diagrams. All channels have bit error ratios (BERs) below the FEC limit of 2×10^{-3} (7 % overhead); no error was detected within the 10 million recorded bits for channel 1 and 3. The high BER of channel 2 can be attributed to the reduced performance of the corresponding amplifier. While the individual plasmonic modulators feature an electro-optic bandwidth > 70 GHz [9], the electrical wire bonds with lengths of ~ 2.5 mm introduce an electrical bandwidth limitation at higher data rates.

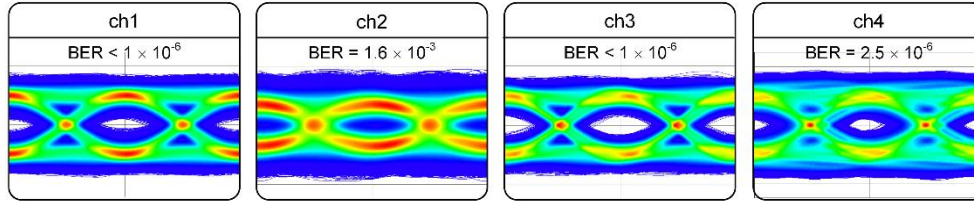


Fig. 2 Transmitter optical eye diagrams with bit error ratios (BER) of the data experiments (BPSK) at data rates of 10 Gbit/s. All four channels have a BER below the FEC limit of 2×10^{-3} .

3. Receiver

To make the optical to electrical signal conversion, a Ge waveguide photodetector (PD) array of IMEC's fully integrated silicon photonics platform with a 50 μm spaced optical interface was used [10]. The detectors were wire bonded to a 4-channel trans-impedance limiting amplifier (TIA) array on an evaluation board, see Fig. 3. To minimize the length of the wire bonds, the photonic chip was diced close to the contact pads and placed in proximity to the electronic chip. One channel could not be bonded, though, since the arrangement of the anode and cathode contact pads on the optical and the electronic chip did not match.

To test the performance of the receiver data reception experiments were performed. Data encoded onto an optical carrier by an external GaAs modulator (20 Gbit/s, NRZ, rectangular, DBBS 15, $\lambda = 1550$ nm) was used to characterize the three working channels of the receiver sequentially. To do so, the modulated light was coupled to the individual channel using a SMF and GCs. The signal quality was evaluated using a digital communication analyzer. A bias voltage of -2 V was applied to the Ge PDs, while the receiver settings were optimized for high quality factors Q^2 of the received eye diagrams. Fig. 4 depicts open optical eye diagrams and quality factors of the investigated channels.

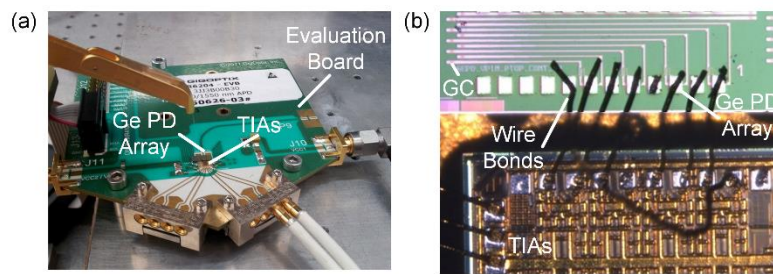


Fig. 3 Receiver (Rx). (a) Evaluation board with Ge PD array and TIAs. (b) Ge PDs wire bonded to the TIAs. One channel could not be bonded, since the arrangement of the anode and cathode contact pads on the optical and the electronic chip did not match.

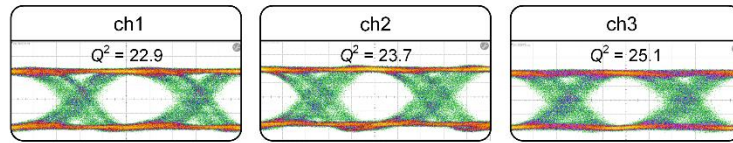


Fig. 4 Receiver optical eye diagrams with quality factor (Q^2) of the data experiments at 20 Gbit/s. The three channels show open eye diagrams.

3. Chip-to-Chip Interconnect

In a final step, transmitter and receiver were tested as a complete chip-to-chip interconnect using the setup shown in see Fig. 5(a). Each optical channel was tested separately. Channel 1 operated at 20 Gbit/s with a BER of 3.3×10^{-5} , see Fig. 5(b). The complete chip-to-chip interconnect operated at 3×10 Gbit/s with BERs of 8.8×10^{-6} , 4.3×10^{-4} and 2.2×10^{-4} as shown in Fig. 5(c).

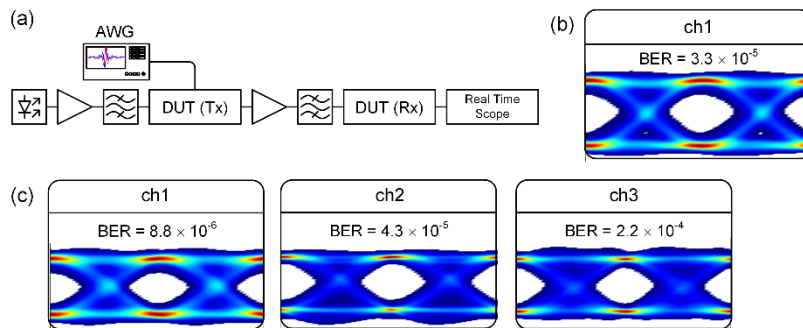


Fig. 5 (a) Experimental setup for data modulation experiments of the complete chip-to-chip interconnect. Laser light at $\lambda \approx 1550$ nm was coupled to the transmitter shown in Fig. 1. Electrical data streams were generated by an arbitrary waveform generator (AWG) and sent to the channel under test of the transmitter. The modulated signal was amplified and sent to the receiver (see Fig. 3). At the receiver output, eye diagrams and bit error ratios were measured with a real time scope and standard digital signal processing. (b) 20 Gbit/s modulation (NRZ, rectangular, DBBS 15) for channel 1. (c) Optical eye diagram and BER of the data experiment at data rates of 10 Gbit/s for all channels.

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